Amendments to the Drawing

In Fig. 6, "no change" has been changed to --change--.

In Figs. 33(a) to 33(d), one of the drawings originally shown was not labeled, and the locations of Figs. 33(b) to 33(d) were incorrect. Therefore, the locations of Figs. 33(b) to 33(d) have been corrected, and label of Fig. 33(e) has been added.

The marked up drawings (Fig. 6 and Figs. 33(b) to 33(d)) and replacement sheets thereof are attached herewith.

Remarks

Reconsideration and allowance of this application, as amended, are respectfully requested. Drawing Figs. 6 and 33(b)-33(e) and claim 3 have been editorially amended. New claim 14 has been added. Claims 1-14 are now pending in the application. The rejections are respectfully submitted to be obviated in view of the amendments and remarks presented herein. No new matter has been introduced through the foregoing amendments.

Fig. 6 has been amended to correct a translation error. An annotated marked-up drawing is presented herein at page 2. Support for the revision is found in the disclosure at, for example, specification pages 21-22, paragraphs [0067] and [0068].

In regard to Figs. 33(a) to 33(d), although five drawings are shown in one sheet, labels of Figs.33(a) to 33(d) were indicated. Figs. 33(a) to 33(e) should be labeled.

In accordance with 37 CFR § 1.121, replacement drawing sheets for Figs. 6 and 33(a)-33(e) are attached hereto.

Entry of each of the amendments is respectfully requested.

35 U.S.C. § 102(b) - Tateishi

Claims 1 and 2 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,912,552 to Tateishi. The Office Action (page 2, paragraph no. 2) asserts in pertinent part that "Tateishi discloses claimed invention a DC-DC converter (figure 1-5 and 7-8), including . . . a means for a first feedback and a second feedback" and "a control mode."

The rejection under § 102(b) is respectfully traversed. For at least the following reasons, the disclosure of Tateishi does not anticipate Applicant's claimed invention.

Applicant's invention is directed to a DC-DC converter for switching a semiconductor switch device to convert a DC voltage

to a certain level and for supplying the DC voltage to a load. Specifically, the invention relates to a DC-DC converter that reduces a switching loss of the semiconductor switch device even when an output voltage fluctuates.

An object of the invention is to provide a DC-DC converter in which overshooting of the output voltage signal does not occur even when the output voltage control signal changes in a stepwise manner.

A further object of the invention is to provide a DC-DC converter in which undershooting and overshooting are suppressed during switching between the PWM control mode and the PFM control mode, so as to minimize absolute values of the overshooting and the undershooting. It is also possible to shorten the periods of the overshooting and the undershooting.

Claim 1 defines a DC-DC converter that includes "control mode selection means connected to the providing means for selecting one of the first feedback control mode and the second feedback control mode, said control mode selection means selecting the second feedback control mode when a load current flowing through the load is below a predetermined value, and selecting the first feedback control mode irrespective of the load current when the second DC voltage supplied to the load changes."

Tateishi also is directed to a DC-DC converter. See, e.g., the disclosure at col. 3, lines 42-55, of a "switching voltage regulator." Tateishi discloses (col. 3, line 55, through col. 4, line 6) that

> In accordance with the invention, the switching control circuit comprises means for monitoring a voltage provided to the output terminal and for generating a first feedback signal which indicates a target inductor current for providing the regulated voltage

> to the output terminal, and driving means responsive to the first feedback signal for selectively supplying driving pulses to the switching means so as to control duty cycle switching of the switching means. The frequency of the switching is varied by the switching means by an amount proportional to a load current. This is possible because the switching means is turned ON by waiting for two set (ready) signals to both become ready. One of the set signals represents a predetermined time constant, while the other set signal represents a time constant according to the load condition. *Since the first feedback signal is used to control the duty cycle and to determine light load conditions*, no error caused by current and voltage offsets is introduced into the determination. Also, a light load threshold may be set more accurately (emphasis added).

In addition to the first feedback signal, Tateishi also discloses (col. 4, lines 7-33) a second feedback signal:

> In a preferred implementation of the invention, the driving means comprises means for monitoring an inductor current output by the inductor to the output terminal and for generating a second feedback signal which indicates the inductor current. Gating means are provided which are responsive to first, second, and third control signals for outputting the switching control signal to close the switching means when the first and second control signals are active and for outputting the switching control signal to open the switching means when the third control signal is active. A pulse generating means provides the first control signal to the gating means, while the third control signal is provided to the gating means in response to the first and second feedback signals, where the third control signal is active when the second feedback signal has a greater value than the first feedback signal. Finally, means are provided which are

> responsive to the first feedback signal for providing the second control signal to the gating means, where the second control signal is inactive when the first feedback signal has a value less than a predetermined value indicative of a light load. *In short, the first control signal from the pulse generating means is only provided to the driving circuitry for the switching means when the target peak current for the regulated voltage exceeds a value indicative of a normal load;* for lighter loads, the second control signal instead of the first control signal determines the timing of turning ON the switching means (emphasis added).

See also the disclosure at col. 6, lines 51-58, where Tateishi discloses that

> Two feedback paths are provided in the voltage regulator circuit in accordance with the invention. *In the first feedback path, a first feedback signal, V_{cnt1}, representing the target peak inductor current for the regulated voltage, is generated by comparing the detected output voltage V_{FB} detected across the voltage divider comprising resistors R_1 and R_2 with a reference voltage V_{REF} using differential amplifier 58* (emphasis added).

Tateishi does, therefore, disclose a first feedback signal and a second feedback signal (see also Tateishi Fig. 5). But, as is evident from the above-quoted disclosure, Tateishi's converter is different from Applicant's claimed converter. In Tateishi, the first feedback signal, V_{cnt1}, which represents the target peak inductor current for the regulated voltage, is generated by comparing the detected output voltage V_{FB} detected across the voltage divider comprising resistors R_1 and R_2 with a reference voltage.

Applicant's claimed converter is different from Tateishi's converter. Tateishi's first feedback signal represents a target peak inductor current for the regulated voltage. In Applicant's claimed converter, the control mode selection means selects the first feedback control mode irrespective of the load current when the second DC voltage supplied to the load changes.

Tateishi, therefore, does not meet Applicant's claimed control mode selection means limitation.

Since Tateishi does not describe each limitation of the claimed invention, Tateishi does not anticipate the invention defined by Applicant's claim 1.

Claim 2 is allowable because it depends from claim 1, and for other reasons. Claim 2 defines a converter in which "said first feedback control mode is a pulse width modulation control mode, and said second feedback control mode is a pulse frequency modulation control mode."

Tateishi fails to disclose a converter meeting both the control mode selection means limitation of claim 1, and the additional PWM and PFM limitations of claim 2.

For at least the above reasons, reconsideration and withdrawal of the rejection of claims 1 and 2 under § 102(b) are respectfully requested.

<u>35 U.S.C. § 103(a) - Kanouda in combination with Katayama</u>

Claims 3-13 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,489,756 to Kanouda et al. (hereinafter "Kanouda") in combination with U.S. Patent No. 6,469,483 to Katayama. The Office Action (page 3, paragraph no. 4) acknowledges that "Kanouda et al. does not disclose the utilization of the technique for an analog amplifier circuit," and relies upon Katayama for "the utilization of the similar technique

for an analog amplifier (figure 1)." The Office Action concludes that "[i]t would have been obvious . . . to modify Kanouda et al.'s DC-DC converter circuit by utilizing the technique taught by Katayama for the purpose of increasing efficiency of the converter."

The rejection of claims 3-13 under § 103(a) is respectfully traversed. The claimed invention would not have been obvious because there is no suggestion or motivation in either Kanouda or Katayama that would have led one to select the references and combine them in a way that would produce the invention defined by any of claims 3-13.

Claim 3 defines a DC-DC converter that includes "control mode selection means connected to the control means for selecting one of the pulse width control mode and the pulse frequency modulation control mode, said control mode selection means selecting the pulse frequency control mode when a load current flowing through the load is below a predetermined value, and selecting the pulse width modulation control mode irrespective of the load current when the second DC voltage supplied to the load changes."

Kanouda is also directed to a DC-DC converter. See, in general, the disclosure at col. 2, line 13, through col. 3, line 37. At col. 2, lines 13-22, Kanouda discloses that

> An object of the present invention is to solve a problem that in a DC-DC converter, the efficiency reduces in a light load area or an area having a large difference in output voltage.
>
> The present invention reduces the control loss by the PWM control, PAM switch control, or linear regulator control depending on the load condition or by controlling the output voltage by switching the PWM control, PAM switch control, or linear regulator control.

Kanouda discloses (col. 6, lines 25-56) that

> In the PWM control, when the output current Iout decreases, thereby the load factor decreases, the output voltage Vout is likely to increase, so that the error voltage signal output from the output feedback circuit 7 is reduced in number and the pulse width of the pulse train signal for driving between the gate and the source of the channel P power MOFET2 is narrowed in correspondence with it. As a result, as shown in FIG. 3, the VD pulse width which is the width of the pulse voltage appearing at both ends of the diode 3 is narrowed as the load factor reduces. However, in the rated load area, the peak value of the VD pulse is fixed.
>
> In the PWM control, the minimum ON pulse width which is a minimum value of the VD pulse width is determined by the limiter 93 and when the load factor reduces to the neighborhood of the minimum ON pulse width, the PWM control is switched to the PAM switch control indicated below, which controls the output voltage. Switching to the PAM switch control is realized by deciding the load condition by the control characteristic control circuit 52 on the basis of the load current detection signal input from the load current detector 51 and switching the change-over switch 12b to the contact A connection condition with the contact A connection condition of the change-over switch 12a kept when the area is changed to the intermediate load area.
>
> By doing this, the output of the amplifier 11 is input to the multiplier 13 and multiplied by the pulse train which is the output of the comparator 92. As a result, the output of the multiplier 13 becomes a pulse train with the minimum ON pulse width whose peak value is changed according to the error voltage signal output from the output feedback circuit 7.

In view of Kanouda's control mode, Kanouda's converter is different from Applicant's claimed converter. Thus, in addition to the deficiency acknowledged in the Office Action, Kanouda fails to suggest, *inter alia*, Applicant's claimed control mode selection means capable of "selecting the pulse width modulation control mode irrespective of the load current when the second DC voltage supplied to the load changes."

Secondly, Katayama does not rectify the above-described deficiencies of Kanouda. Katayama is directed to a PWM control circuit for a DC-DC converter. Katayama discloses (col. 2, lines 20-36) that

> To attain the above object, the first aspect of the present invention provides a PWM control circuit for a DC--DC converter comprising a detection circuit for detecting an output voltage from a DC--DC converter that converts one DC voltage into another DC voltage by turning on and off a semiconductor switch, an error amplification circuit for amplifying a difference between the detected voltage and a reference voltage, and a comparison circuit for comparing an output voltage from the error amplification circuit with a carrier signal with a triangular wave or saw-tooth wave, and generating a PWM signal that drives the DC--DC converter. In the invention, the error amplification circuit is configured by cascading together a first analog amplification circuit having a fixed operation point, and a second analog amplification circuit having a fixed operation point, and the first analog amplification circuit is a differential amplification circuit.

Thus, Katayama may disclose an amplification circuit, but fails to suggest anything whatsoever related to Applicant's claimed control mode selection means.

Therefore, the claimed invention would not have been obvious because there is no suggestion or motivation in either Kanouda or Katayama that would have led one to select the references and combine them in a way that would produce the invention defined by any of claims 3-13. The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination.

Claims 4-13 are allowable because they depend from claim 3, and for other reasons. Each of claims 4-13 depends, either directly or indirectly, from claim 3, and adds additional limitations not met by Kanouda and Katayama, either alone or in combination.

For at least the above reasons, reconsideration and withdrawal of the rejection of claims 3-13 under § 103(a) are respectfully requested.

New claim 14 is also allowable. Claim 14 defines a converter that includes "means for providing a first feedback control mode that is a pulse width modulation control mode," and control mode selection means "capable of selecting the first feedback control mode irrespective of the load current when the second DC voltage supplied to the load changes." None of the references of record either anticipates or would have rendered obvious the converter defined by new claim 14.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the examiner is respectfully requested to withdraw the outstanding rejection of the claims and pass this application to issue.

Respectfully submitted,

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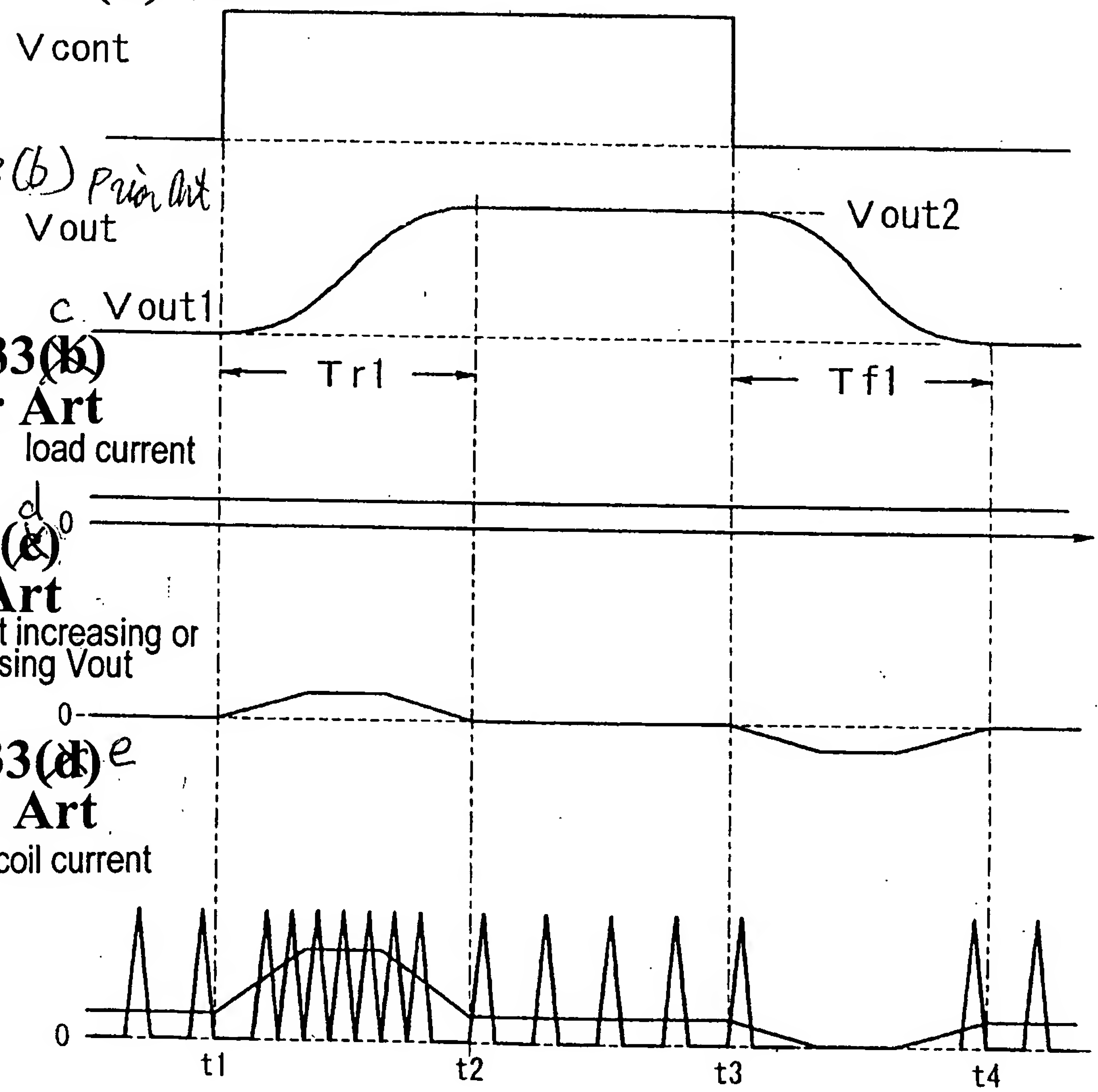
Fig. 33(a) Prior Art



Fig, 33(b) Prior Art

Fig. 33(~~b~~ c) Prior Art

Fig. 33(~~c~~ d) Prior Art

Fig. 33(~~d~~ e) Prior Art

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Fig. 6

output voltages / load conditions	no change (req2=Low)	~~no~~ change (req2=High)
light load (req1=Low)	PWM/PFM =Low	PWM/PFM =High
heavy load (req1=High)	PWM/PFM =High	PWM/PFM =High